Amplifier Efficiency Enhancement Through Dynamic Bias Switching

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Abstract: *Linear digital modulation techniques in modern communication systems introduce a higher peak-to-average ratio to their signal envelope. For linear amplification of such signals, the power amplifier must be operated at excessive (7 – 10 dB) back off, thus sacrificing overall amplifier efficiency. To enhance the efficiency of the amplifier without degrading spectral re-growth (intermodulation products), a Dynamic Bias Switching (DBS) system has been implemented -This is achieved by partitioning the required supply rail into two or more levels. The supply voltage is switched between the steps, and is adjusted in accordance to the signal envelope. This is accomplished by using a pass-transistor (gate) operated as a switch with very low channel resistance. This approach avoids the energy loss associated with continuous tracking (amplification) of the signal envelope reported in the literature.*

Keywords: Dynamic Bias Adjustment, Envelope Clipping, and Digital Modulation Amplification

1.0 BACKGROUND

The growth in cellular communication use, coupled with increased frequency congestion and limited available air-interface bandwidths, has led to stringent specifications for the transmitters. In particular, the base-station power amplifiers must have excellent linearity to minimize the out-of-band emissions, and allow for frequency re-use schemes.

Several alternative approaches have been proposed to circumvent the problem outlined above. Radio Frequency (RF) PAs are highly nonlinear but efficient when operated in compression. However, the amplifier non-linearity can be tolerated if the input signal has a constant envelope. Examples of this are single carrier frequency modulated (FM) signals and Gaussian Minimum Shift Keying (GMSK) used in GSM cellular communication standards. The information carrying capacity of these non-linear modulation schemes is limited. Lately more bandwidth-efficient digital modulation schemes such as quaternary phase-shift keying (QPSK) and 8-PSK are being used. In most of these schemes, even though the information is only embedded in the carrier phase, a relatively large amplitude variation (or signal envelope) is also present. In order to control amplitude distortion and out of band emissions, the PA has to be able to cope with the frequent signal peaks, while on average, the signal amplitude remains considerably lower.

Among various alternatives proposed, some simply attempt to clip the signal peaks. The drawback with clipping is that it will increase the bit error rate (BER) and the spectral regrowth or the out-of-band emissions. Envelope elimination and restoration (EER) known as Kahn technique is, however, an elegant solution [1]-[2].

In this system, the RF input signal is decomposed into a low frequency envelope signal and a constant envelope phase modulated RF carrier. This is done by applying a sample of the RF input carrier to an envelope detector prior to removing the envelope by means of a hard limiter. The output of the limiter will have a constant envelope and only phase-bearing information. The conversion of the input signal into a polar representation means that in an EER system, the phase-modulated part of the signal and magnitude can be amplified separately. An efficient non-linear amplifier of Class-C, E or Class-F can be used for the phase-modulated constant envelope signal. A switching power supply (SPS) amplifies the envelope information. In the reconstruction process, the output of the SPS modulates the supply voltage of the PA, to recover the original envelope. The depth of modulation is monitored and adjusted by providing a feedback path from the output to the input of the switching power supply.

The efficiency of the Kahn amplifier comes at a penalty in terms of IMD. The sources of added non-linearity are: the Class-S modulator, the amplitude modulation (AM) linearity of the RF PA, the differential delay between the envelope amplification path and the RF amplifier and more importantly, the bandwidth of Class-S modulator [4]. As a rule of thumb, the intermodulation distortion (IM) can be kept below –30dBc if the $B_S \geq 1.78\ B_{RF}$', where B_S is the bandwidth of the modulator and B_{RF} is the bandwidth of the RF signal [2]. A Class S-modulator is similar to a switching mode dc-dc switching power converter, the major difference being that the Class-S modulator operates with a variable reference signal supplied by the RF carrier envelope. The useful frequency bandwidth of the analogue implementation of EER amplifiers is limited to a few hundred kHz.

In order to circumvent the bandwidth limitation of a Class S-modulator in other variants of this technique, the active device (transistor) is biased dynamically as the signal envelope varies with time. The two techniques considered to be of prior art are by Buoli [3] and an international patent WO 01/67593 A2, [PCT/IL01/00221].

Buoli developed a linear regulator power drive, whereby the V_{DD} (drain voltage) supplied to a final stage of MESFET amplifier is controlled and tracks the RF envelope. Restating the fact that the losses in the RF transistor is given as the quiescent current multiplied by the voltage across the device, in Buoli approach, to improve the efficiency, the voltage applied to the amplifier was obtained from a dual source. A main voltage of +7 V is used until the peak of the signal exceeds a pre-set threshold, and then a second supply is used. A linearly-controlled voltage supply (between 7-12 V) tracks the signal envelope. Although the higher voltage (V_{DDH}) is provided via a relatively inefficient fast video amplifier and a linear pass-transistor, considerable improvement in efficiency was demonstrated [3]. In such a system dc power is saved, since for low levels of envelope, the energy source is provided by the 7-V supply, and the dynamic supply (7-12V) is used only for a fraction of the time. In such an approach, the second supply replicates the signal above the threshold and for this part of the operation; the amplification process is linear and therefore inefficient. The above-mentioned patent (WO 01/67593 A2, PCT/IL01/00221) generalizes the approach mentioned above.

2.0 DBS THEORY OF OPERATION

In the technique described in the current paper, unlike EER or variations of envelope tracking systems which the amplitude modulates the supply voltage, the DBS simply steps up the supply voltage only at moments of signal peaks for a linear operation. As shown in Figure 1, this technique is effective for signals with high peak-to-average ratios.

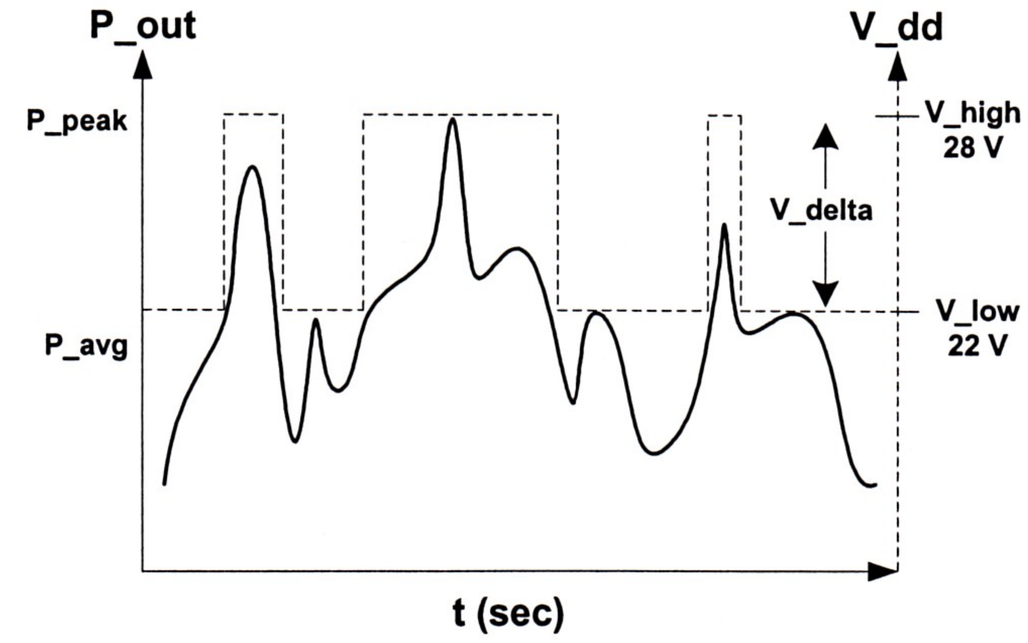

Figure 1: Two Step voltage switching at RF peaks

RF peaks are sampled and detected at a prescribed threshold from the system input. This information is then used by low-loss, high-speed MOSFET drivers and switches to adjust the drain voltage of the RF device at moments of peak. A basic DBS circuit diagram is illustrated in

Figure 2. There is substantial savings in average DC power consumption when the high-power device voltage requirement is lowered significantly (V_main). A smaller voltage source (V_add) would maintain very low, average DC power from occasional peaks. An array of storage capacitance also minimizes peak current demands from the added voltage supply.

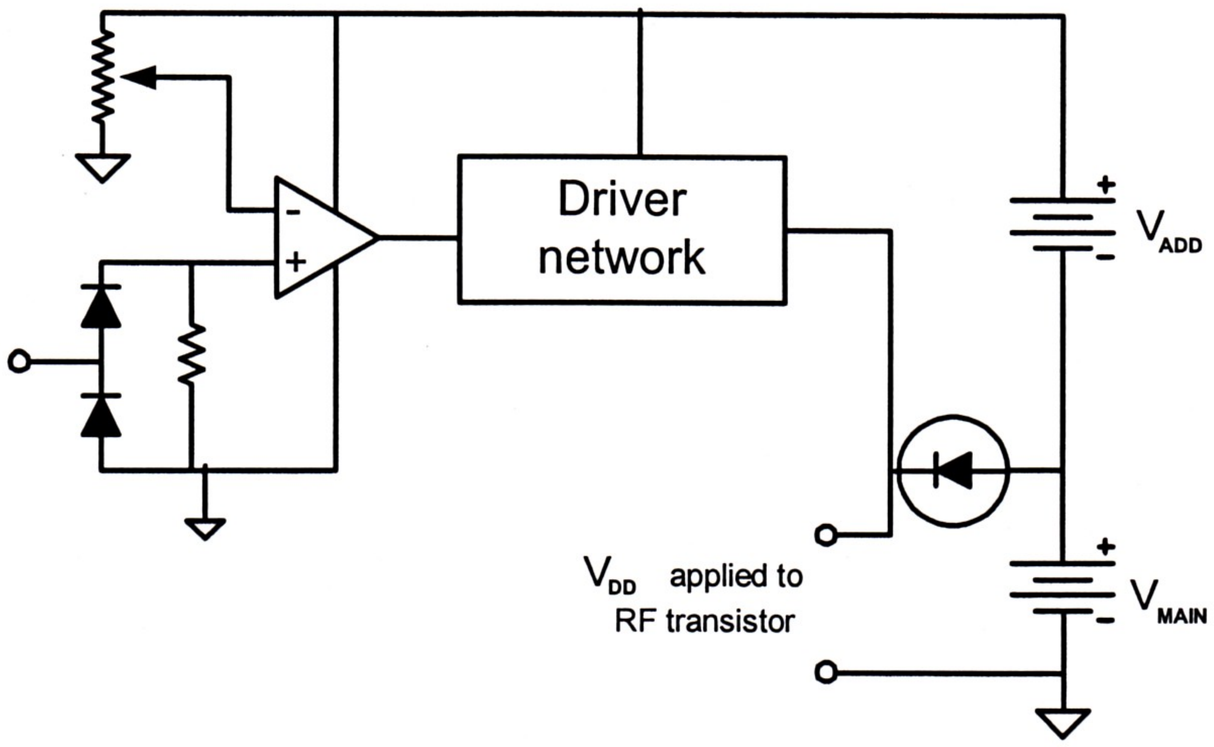

Figure 2: DBS Basic Circuit Schematic

The DBS circuit was implemented in a FFPA (Feed Forward Power Amplifier) development platform with a known efficiency. A block diagram is shown in Figure 3. Inherently, this FFPA exhibits good RF to DC efficiency due to prior enhancements employed to the platform. There is still some room for the DBA to save significant power. The Peak Detector and Switching Regulator components were detailed in

Figure 2.

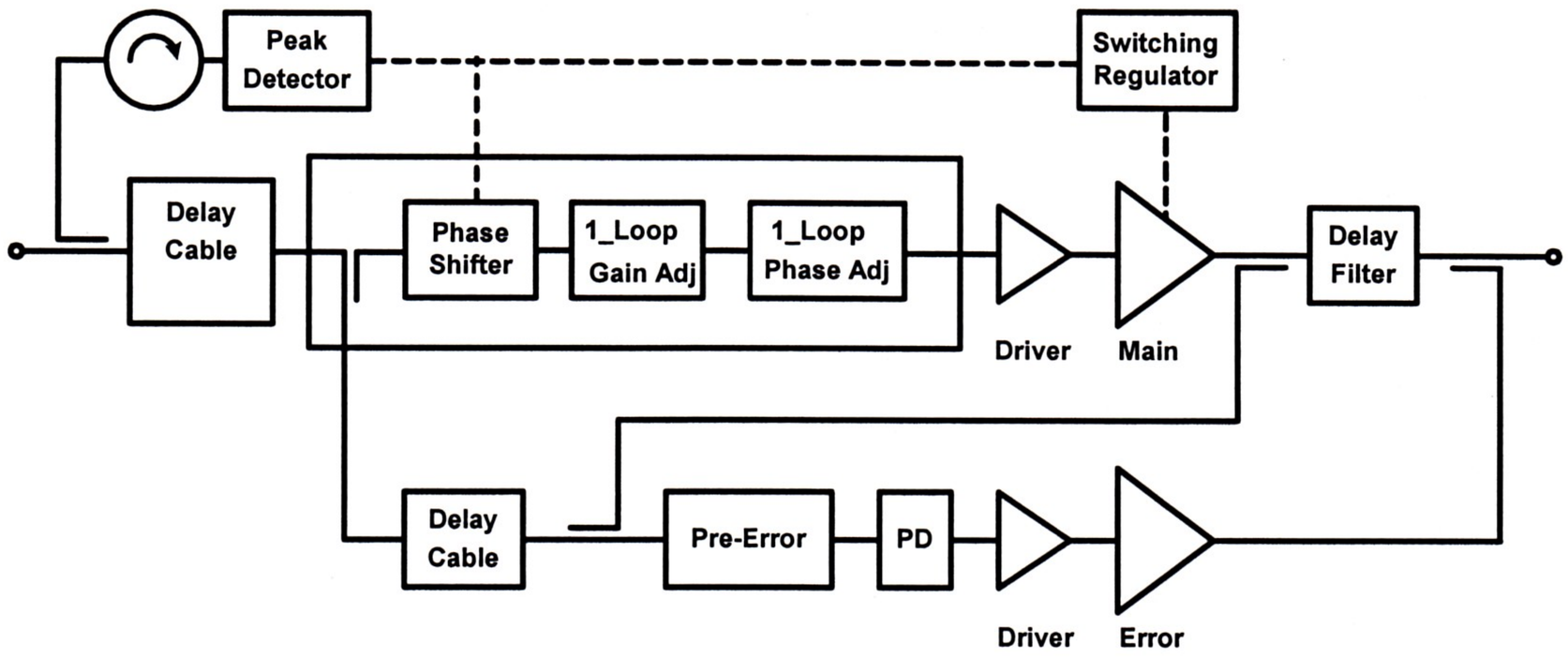

Figure 3: FFPA basic block diagram with DBA

3.0 DBS INTEGRATION

From the onset the DBS experiments were focused on the output stages of the Main Amplifier module. Only these final device stages were switched while the remaining stages were supplied with fixed drain voltages. Toggling the drain at two distinct voltages can vary the device gain magnitude and phase angle.

Consequently, the variation has adverse effects on carrier cancellation at the first loop of the FFPA. Any efficiency improvement from the DBS can be easily lost here if left unchecked. Some un-cancelled carrier power would leak through and increase the Error Amplifier current. In this platform, only the phase swing was large enough to require compensation by means of a simple phase shifter controlled by the peak threshold detector.

Time alignment is crucial between the RF signal peaks and the low frequency switching from detected peaks. A careful reconstruction of the original signal peak at the output stages can lessen the impact of IMDs introduced by delay mismatch, which is given by:

$$IMD \approx 2\pi B_{RF}^{2} \Delta\tau^{2}$$

where B_{RF} is the signal bandwidth and $\Delta\tau$ is the delay mismatch. A low-loss coaxial cable or any other slow wave structure can be used to synchronize the RF and Analog paths.

The total switching speed from peak threshold detection to a steady-state drain voltage level must be fast enough to cover all the envelope peaks occurring throughout the entire RF bandwidth of a digital modulated signal like CDMA. The DBS technique has a bandwidth limitation expressed by:

$$f_S = 1/t_S = \frac{1}{2RF_{BW}}$$

A CDMA signal with a 10 MHz bandwidth must have a system switching speed of no more than 50 nsec so that signal peaks are supplied with enough DC power on demand. Otherwise, a wider signal or a slower switching speed will cause the FFPA to generate elevated distortion products and efficiency would suffer from improper loop cancellation.

The envelope peaks are in effect pulse-modulated at the drain voltage, where the resulting spectral density may add distortion if any part of its side lobes is in-phase with the third and fifth-order IMDs. A smoother, less abrupt pulse shape in the switching mechanism is required to reduce distortion.

4.0 EXPERIMENTAL RESULTS

The FFPA test platform was originally optimized for a W-CDMA two-tone signal in a 15 MHz bandwidth with CCDF=9.5. The ACPR has 5dB margin from industry specifications. The addition of a DBS circuit in the main amplifier module enabled the partitioning of 28V drain supply voltage into 22V and 6V. The table below illustrates the efficiency enhancement to the FFPA system.

Status	RF Power	Supply Voltage	Supply Current	DC Power	Efficiency
Baseline	32 W	28 V	10 A	280 W	11.4 %
Enhanced	32 W	22 V 6 V	10 A 4 A	220 W 24 W	13.1 %
Efficiency Enhancement				36 W	1.7 %

Table 1. Comparison of baseline and enhanced FFPA system

At moments of peak, the additional 6V provides the full 28V required for linear operation. The switched power devices draw a total of 3.9A in a baseline configuration. As shown in Table 1, this current is drawn as well by the 6V supply from the DBS enhanced unit. Note that the infrequent peak power occurrences have negligible current demands from the 6V supply, which is aided by sizable storage capacitors.

Figure 4 is a spectral plot for the baseline FFPA output with a fixed +28V power supply. These results are compared to the performance of a FFPA with DDA enabled in Figure 6 depicting carrier-cancelled outputs through a Dynamic Range Extender (DRE). The ACPR measurements are absolute values in dBm, which are referenced from one channel power at one-half the total Pout as measured when DRE is disabled. The significant ACPR measurement is labeled ALT2 Upper.

Waveform CCDF = 9.5dB

Pout = 45 dBm (32W)

Vs = 28V

Total Watts = 280W

Efficiency = 11.2%

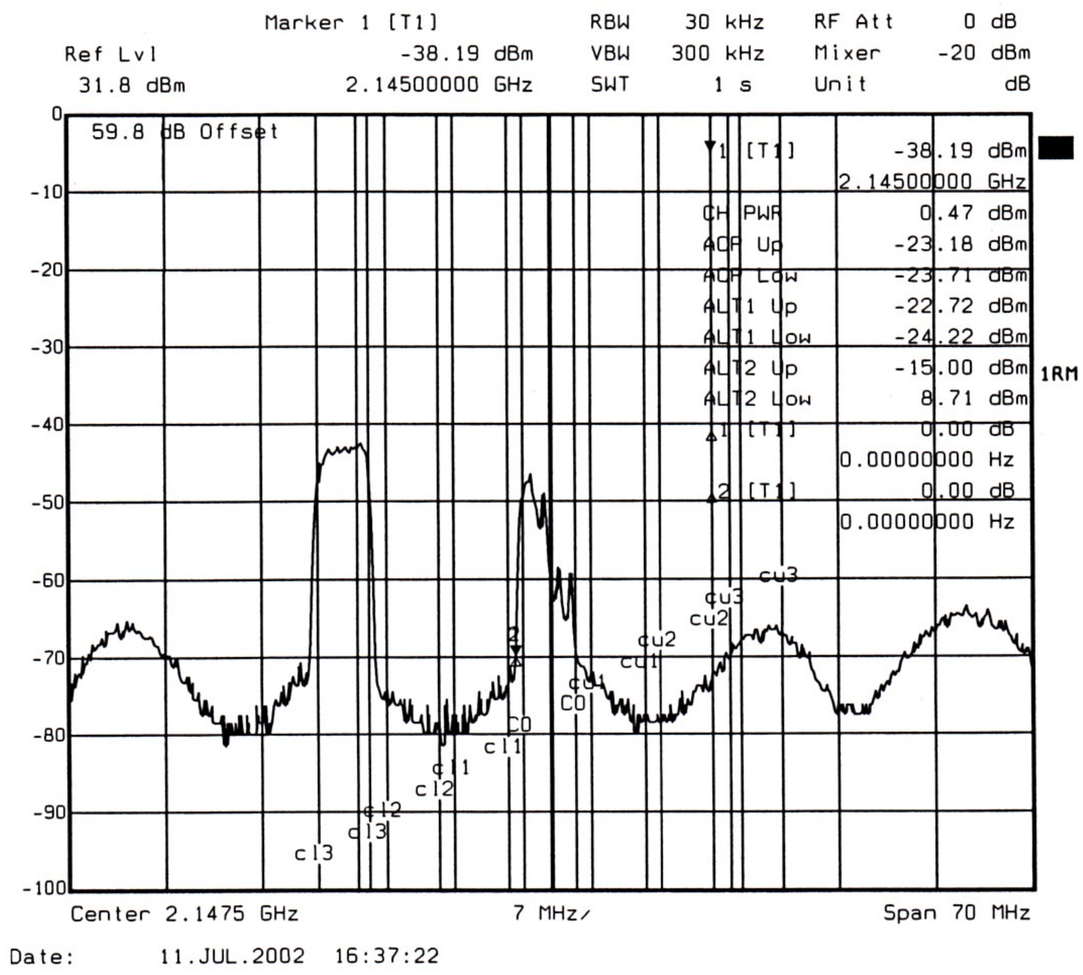

Figure 4: Baseline FFPA performance at 28 Vdc

Waveform CCDF = 9.5dB

Pout = 45 dBm (32W)

Vs = 22V

Vd = 28V

Total Watts = 244W

Efficiency = 13.1%

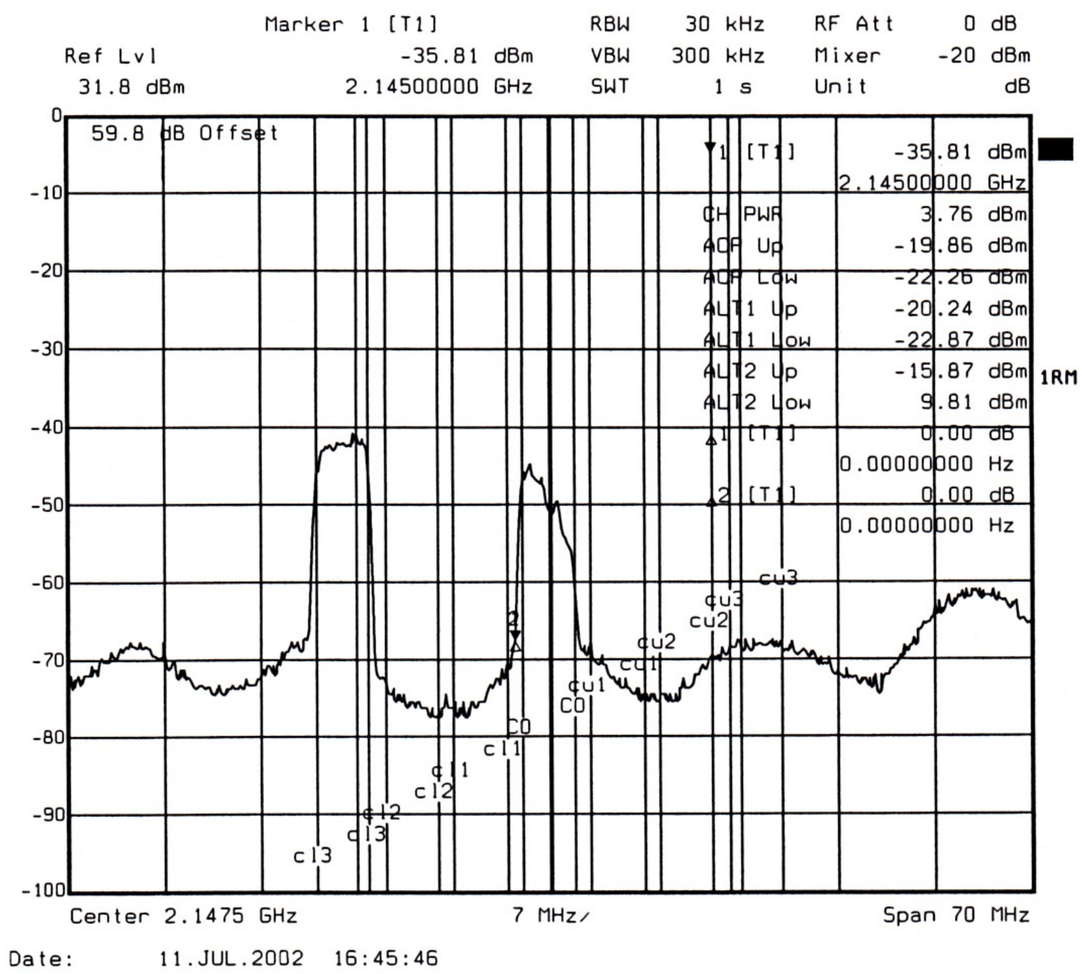

Figure 5: FFPA with DDA enabled

5.0 THE IMPACT OF SIGNAL STATISTICS

When optimizing amplifier performance, the drain voltage spread (V_delta, step size) of a two-step supply tends to narrow down as the crest factor of RF signal decreases. This is shown in Figure 6. A smaller voltage spread does mean a lower power savings. On the other hand, a signal with a low crest factor can achieve greater average output power on the same PA than of a higher one. This makes the DBA a competing technology to crest factor minimization techniques.

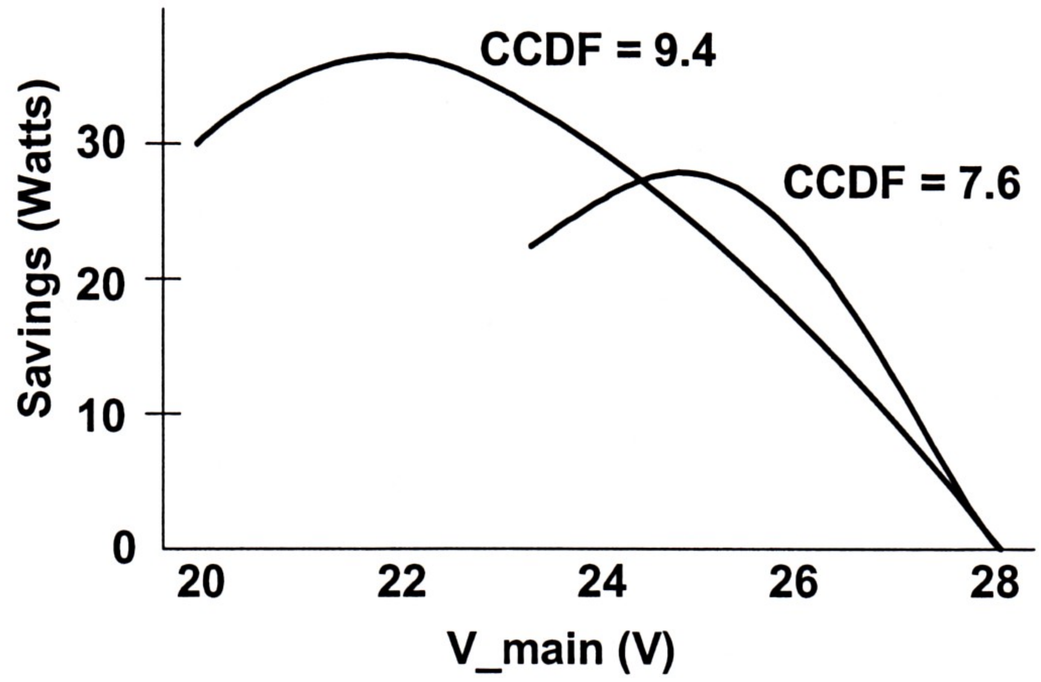

Figure 6: Efficiency improvement of high & low crest factor

6.0 CONCLUSION

A practical application of the DBS technique is presented with some improvement in efficiency, and technical issues associated with the FFPA integration as was discussed. Efficiency and spectral performance are affected by uncompensated gain and phase fluctuations, delay mismatches from RF and low frequency switching, sampling speed and shape, and system noise through interconnections. Without the proper attention to such issues, the Error Amplifier would be more at risk to reduce efficiency enhancements gained by the Main Amp and unwanted IMD regrowth would not justify the use of this technique. The DBS is also appropriate when used in conjunction with other efficiency boosting methods.

REFERENCES

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