On the Effects of the Average Power of Training Sequences Used to Synthesize Memory Digital Predistorters in WCDMA Transmitters

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***Abstract*— In this paper, a study of the effects of the average power of the training sequences used in characterizing the power amplifier on the performance of synthesized memory polynomial digital predistorters is presented. This study was carried out on a 3G 100-Watt peak power amplifier operating over a 12 dB average input power range. The amplifier was characterized over this power range in steps of 1 dB, and the corresponding memory polynomial predistortion function was derived at each operating average power. It was shown that the average power mismatch between the power amplifier and the predistorter degraded the adjacent channel power ratio of the linearized amplifier by up to 9 dB. The predistorter's parameters variation with the average input power was then investigated. Consequently, a nonlinear filter bank was proposed to store the memory polynomial coefficients as a function of the average power levels. The memory bank is added to the predistorter along with an average power estimator, in order to maintain the performance of the linearized amplifier over the entire input power range.**

I. Introduction

Various wireless communication standards are being deployed in order to offer worldwide ubiquitous wireless coverage with both voice and data transmission services. To achieve the targeted high data throughput within the limited and overcrowded radio frequency (RF) spectrum, highly spectrum-efficient access techniques based on code division multiple access (CDMA) and orthogonal frequency division multiplexing (OFDM) are used. Such techniques result in envelope varying signals that have high peak-to-average power ratio (PAPR). These signals set stringent linearity and power efficiency requirements on the RF front end. At the transmitter side, the RF power amplifier (PA) is the most critical subsystem that predominantly contributes to the transmitter's nonlinearity and power efficiency. Indeed, when driven by high PAPR signals, brute force power amplifiers are unable to achieve the required linearity that satisfies the spectrum emission mask with acceptable power efficiency. This is mainly due to the PA's inherent linearity versus power efficiency dilemma. Two approaches are being considered to meet the linearity requirements with the highest possible power efficiency. The first approach consists of using a continuously driven PA in conjunction with a linearization technique [1]-[3]; while the second one is based on the use of switching mode amplifiers within advanced amplification architectures, such as: linear amplification using nonlinear components (LINC), envelope elimination and restoration, and envelope tracking [3]-[6]. The first approach is currently being considered for production and deployment in wireless infrastructure, while the second one is still in the research and development phase.

Several linearization techniques have been reported in the literature [1]-[3]. Among these techniques, the digital predistortion is the most suitable for base station applications. Indeed, in comparison with feedforward linearizers, digital predistorters present a lower complexity scheme and result in higher power efficiency, while meeting the linearity requirements. However, contrary to the feedforward technique, which is a closed loop technique, digital predistortion is an open loop technique that requires accurate characterization of the PA's behavior [7]. In fact, the linearity performance of the linearized amplifier is greatly dependant on the match between the applied predistortion function and the complementary nonlinearity of the actual PA's characteristics. Thus, it is essential to use an adequate signal at the characterization step, so that the behavior of the PA does not change once the derived predistortion function is applied.

In [7], it was shown that PA behavior depends on the type of driving signal. Moreover, it was demonstrated that, for a given signal type and statistics, the PA behavior depends on the average power level [8]. This dependency was quantified in the case of a 3G power amplification line-up driven by multi-carrier WCDMA signals and having an average power varying over a 12 dB range. In such conditions, the spectrum estimation error, which is the difference between the estimated PA's output spectrum and the actual PA's output spectrum, under average power mismatch was found to be up to 4 dB. Such an estimation error may translate into more important linearity degradation when memory polynomial predistorters that have been derived under average power mismatch are considered. Herein, the average power mismatch refers to the variation of the PA's operating average power between the steps where the PA is characterized and linearized. In practical conditions, the average power mismatch may result from a change in the average power of the transmitted signal or from the introduction of the predistortion function.

In this paper, the effects of the average power of the training sequences used in characterizing the power amplifier on the performance of the linearized amplifier are quantified. The dependency of the memory polynomial based predistorter on the average input power was also studied. In Section II, the experimental setup is presented along with the effects of the average power mismatched characterization on the PA model accuracy. The linearity performance of the linearized PA is then quantified under average power mismatched characterization conditions in Section III. The variation of the predistorter's parameters with the average input power is investigated in Section IV, and the conclusions are presented in Section V.

II. Effects of the Average Power Mismatched Characterization on the PA's Model Accuracy

The device under test (DUT) considered in this work was a 100-Watt peak power amplifier that was driven by a 3-carrier WCDMA signal having a total bandwidth of 15 MHz and a PAPR of 10.6 dB. The complex gain of the PA was extracted from the measured instantaneous input and output waveforms over a wide range of input power drive levels. The average power of the training sequence at the input of the PA was varied from −3 dBm to −14 dBm in steps of 1 dB. The characterization was performed for each of these power levels. The parameters of a 3-branch memory polynomial model were identified for each measurement set.

The model's accuracy in predicting PA behavior under average power mismatch was evaluated. This consists of comparing the spectrum at the output of the PA, operating at a given average power level, with the estimated spectrum at the output of the PA model that was derived from a training sequence having a different average power level. In both cases, the PA and the model were driven by the same type of signal. Fig. 1 presents the model's spectrum estimation error (at 15 MHz away from the carrier frequency) under average power mismatch. Each of the curves presented in this figure corresponds to a constant average power drive level at the input of the PA. Accordingly, the spectrum estimation error increases as the average power mismatch increases between the model and the actual PA operating condition; however, the estimation error is limited to 4 dB. A more detailed study of the effects of the average power mismatch on the model accuracy was reported by the authors in [8].

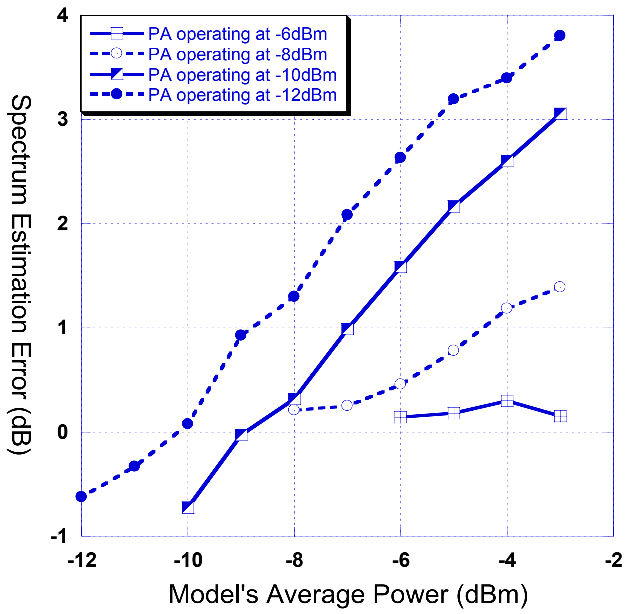

Fig. 1. Spectrum estimation error under average power mismatch

III. Performance of the Linearized PA Under Average Power Mismatched

The DUT characterization performed over the 12 dB input power range was also used to derive the corresponding memory polynomials based predistorters at each operating power level. A 3-branch memory polynomial function was used; and, for each branch, the polynomial order was set to 12. The digital predistorter (DPD) was implemented in Agilent's Advanced Design System software, and the predistorted baseband waveform was downloaded into an arbitrary waveform generator that fed the DUT the corresponding RF signal.

The predistorters were then used to linearize the power amplifier under various power drive levels. The measured adjacent channel power ratio (ACPR) at the output of the linearized PA for an average input power level of −12 dBm is reported in Fig. 2. In this figure, the DPD's average power refers to the average input power level of the training sequence used to derive the predistortion function. According to this figure, the best ACPR performance is obtained when the actual average input power level applied to the power amplifier is equal to that used during the characterization step that led to the synthesis of the predistortion function. In addition, as the power mismatch between the characterization step and the linearization step increases, a more pronounced degradation in the linearized PA's ACPR is observed. This degradation between the best and the worst case is around 9 dB for the ACPR measured at 10 MHz and 15 MHz away from the carrier frequency. However, the effect is less pronounced for the ACPR measured at 20 MHz away from the carrier frequency. This can be attributed to the nonlinearity order of the DUT. Similar results were obtained under different input power drive levels for which the best ACPR performance was obtained when the PA drive level was equal to the drive level used to derive the predistortion function. Moreover, these results highlight that the predistorter's sensitivity to the average power mismatch is more pronounced than that of the PA model.

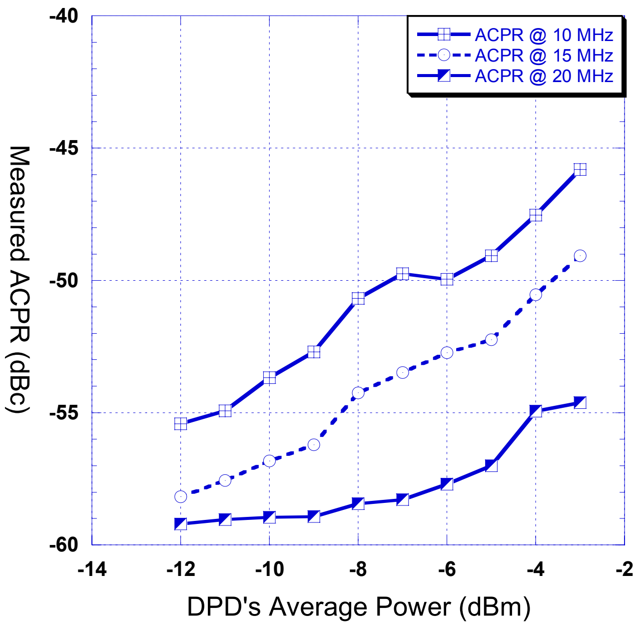

Fig. 2. Measured ACPR vs. DPD's average power ($P_{in,avg} = -12$ dBm)

IV. Memory-Polynomial DPD with Embedded Average-Power Dependency

The performance of the linearized PA under average power mismatch calls for the tracking of the PA behavior dependency with the average input power and update of the predistortion function, in order to maintain the linearity performance of the linearized amplifier. Knowing that the average power variation occurs quickly, the predistortion function update should be performed by loading new DPD parameters that have been precalculated off-line. Thus, additional characterization procedures, which are time and resource consuming, can be avoided. Two approaches have been considered. The first one consists of deriving an analytical function that fits the variation of the DPD parameters with respect to the average input power. The second approach consists of storing the required DPD parameters into a memory bank.

The DPD output signal is given by:

$$y(n) = \sum_{j=0}^{2}\sum_{i=0}^{12} p_{i+1+j\cdot 13} \cdot x(n-j) \cdot \left|x(n-j)\right|^{i} \qquad (1)$$

where $x(n)$ and p_k are the input data sample and the k^{th} coefficient of the multi-branch polynomial, respectively.

First, the variation of the DPD parameters with respect to the average input power was investigated. For this purpose, the normalized real and imaginary parts of the predistorters' coefficients were calculated using (2). Fig. 3 presents the variation of the predistorters' normalized coefficients versus the average input power. Accordingly, one can conclude that these parameters cannot be fitted using a low complexity analytical function.

$$\begin{cases} real\_norm(p_k) = \left| \dfrac{real(p_k)}{\max\limits_{k=1\ldots39}\left(real(p_k)\right)} \right| \\ imag\_norm(p_k) = \left| \dfrac{imag(p_k)}{\max\limits_{k=1\ldots39}\left(imag(p_k)\right)} \right| \end{cases} \qquad (2)$$

Following the previous analysis, a memory bank based approach was chosen to take into account the variation of the predistorters' parameters versus the average input power. The architecture of the augmented predistorter is shown in Fig. 4. One can distinguish three main blocks for this predistorter: the conventional predistorter architecture, an average power estimator, and a memory bank that stores the various predistorters' parameters. The average input power of the signal to be transmitted was estimated using the average power estimator. The estimated power level was used to select, among the different DPD parameters sets stored in the memory bank, the set that corresponded to the actual operating average power. This ensured a continuous power match between the predistortion function and the operating average power level.

V. Conclusions

In this paper, the effects of the average power of the training sequence used to derive memory polynomial based digital predistorters are presented. First, the accuracy of the PA model under average power mismatch was quantified. Then, the linearity performance of the linearized amplifier was evaluated experimentally under average power mismatch. This mismatch degraded the linearity performance by up to 9 dB, which is almost 30% of the linearity improvement achieved by digital predistorters. It has been demonstrated that the best linearity performances are obtained when the average power used to derive the predistorter is equal to that applied to the linearized PA. Subsequently, the variation of the predistorter parameters was investigated as a function of the average input power. It has been concluded that a memory bank based predistorter is more suitable to tracking the PA behavior variation versus the average input power and to keeping acceptable linearity performance over the entire operating power range.

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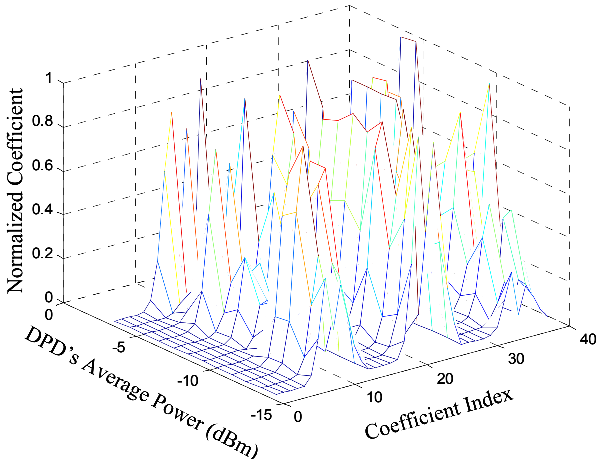
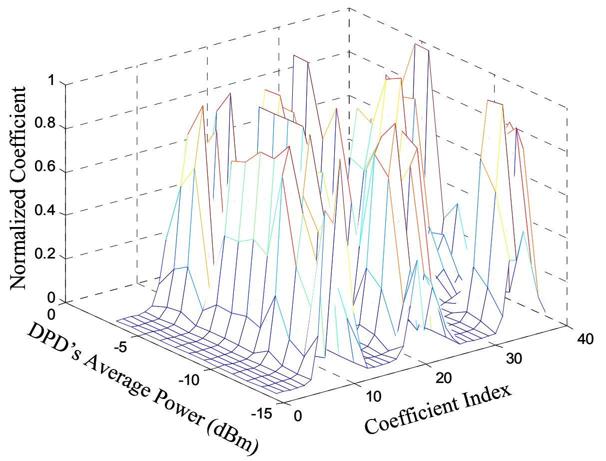


(a)



(b)

Fig. 3. DPDs' parameters variation versus the average input power level. (a) real part (b) imaginary part

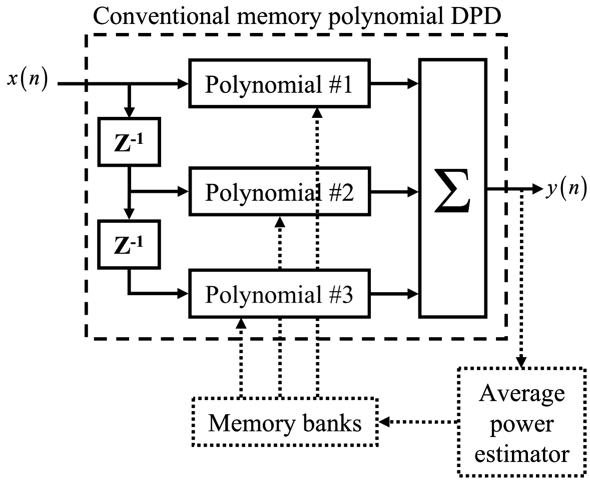


Fig. 4. Proposed memory-polynomial predistorter with average power tracking

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