High Efficiency Base Station Amplifier Architectures Utilizing LDMOS and GaN High Power Transistors

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Abstract

High efficiency amplifier architectures are critical in modern communication systems. Third generation cellular systems and the upcoming LTE (Long Term Evolution) networks will continue to demand increasing transmitter efficiency and lower cost. In addition, linearity demands will be more stringent in order to meet the required spectral efficiencies, and the high bit throughput required by network users.

INTRODUCTION

With each successive generation of commercial cellular system deployment, the architecture of the Base Transceiver Station (BTS) has become more challenging. Figure 1 shows a typical high level block diagram, which contains the amplifier module, the LNA section, the required filtering, and the analog or baseband cards that interface with the rest of the system. In early systems, Single Carrier Power Amplifiers (SCPAs) were employed and the power from many transmitters combined with cavity combiners resulted poor efficiency and high losses. In 2nd and 3rd Generation digital systems, they have been replaced with Multi-Carrier, highly linearized amplifiers (MCPAs). Increasingly, the input to the amplifier block is baseband rather than RF, and the whole assembly has been made more integrated with the other components, and weatherproofed so it can be mounted closer to the antenna as a Remote Radio Head (RRH) in order to achieve lower loss and lower system Noise Figure.

Figure 1. Typical BTS Block Diagram

Figure 2 shows a simplified block diagram of a Feed forward linearized amplifier (FFPA). The error signal (IMD products) is pre-amplified to the required level in the error amplifier chain before extracted (tapped) for feedback. The amplitude and phase of the feedback signal (error) are conditioned prior to the injection at the input of the main amplifier. It is clear that by recombining the feedback components in the main amplifier output, the IMD products can be reduced provided that the correct magnitude and (anti) phase are realized over the desired frequency range. The main and error amplifiers are composed of LDMOS based transistors. A typical 160 W average output FFPA contains a total combined 1120 W of silicon in the main amp, and 380 W in the error amp. This is required due to the high peak to average distribution of the input signal, typically higher than 10 dB. It is easy to see that at about 40 to 50 cents per watt typical transistor cost, the amplifier section of the BTS is easily the most expensive component.

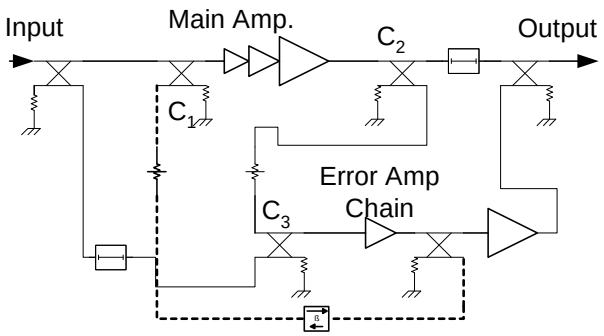

Figure 2. Typical FFPA Block Diagram

Excellent performance has been achieved in the latest designs, unsurpassed by other methods of linearization as shown in Figure 2. Better than 65 dBC intermodulation ratio can be achieved over wide RF bandwidths. In addition, the key performance that has not been achieved with Digital Pre-distortion (DPD) is operation over wide instantaneous bandwidths of input signal of greater than 65 MHz as shown in Figure 2. In addition, the latest designs

are achieving system efficiency, that is, P_{out} /P_{tot} of close to 20%.

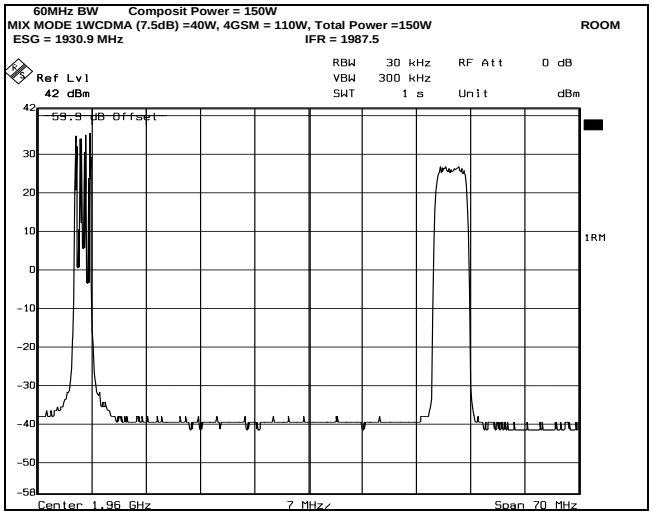

Figure 3. MCPA IMDs Over Wide Instantaneous BW

In DPD and RRH systems, where the amplifier is integrated with the receiver, filtering and digital correction circuitry, similar efficiencies can be achieved, but at lower power, typically 40 W, and lower instantaneous Bandwidth, typically 20 MHz. The advantage of DPD systems lies in the fact that the linearization is achieved digitally; they can be remotely (up to 20 Km) connected to the base station via baseband signaling, and can be mounted as stated previously, much closer to the antenna.

DOHERTY & GATE MODULATION

The Doherty amplifier is well documented and is critical in achieving high efficiency in both FFPA and DPD based RRH solutions where high crest factor signals are employed. The basic concept of the Doherty circuit is to increase the average efficiency by operating a peaking amplifier in Class C and a carrier amplifier in Class AB as shown in Figure 4. Further, the carrier amplifier's load impedance is effectively modulated by input power. The peaking amplifier (biased Class C) is turned on by input RF drive and hence modulates the carrier amplifier's load impedance from high efficiency at low drive levels, to best saturated output at high input drive levels. Modulation of the carrier amplifier's load impedance further increases efficiency of the Doherty circuit. The powers provided by the carrier and peaking amplifiers combine to achieve the full saturated output power from the circuit.

In practice, the peaking amplifier typically does not fully turn on during the peak excursions of the input signal envelope, limiting saturated output power and efficiency. Achieving maximum saturated output power allows the Doherty circuit to be used at higher average output power and increases efficiency.

The simplest technique for improving the saturated output power is to place a small bias on the peaking transistor. Typical peaking amplifier gate bias for LDMOS transistors is 1V, well below pinch off. A second technique that has been well documented is to employ an unequal power split at the input of the Doherty circuit. This unequal split provides higher power to the peaking transistor than the carrier transistor, thus enabling the peaking transistor to turn on at an earlier drive level. This technique decreases the gain of the Doherty circuit and can prove difficult in a manufacturing environment where tuning is required on the input of the carrier amplifier. A third technique is the use of a gate modulator or gate corrector.

Figure 4 depicts a Doherty amplifier with a gate modulator and driver. The gate modulator increases the peaking amplifier gate voltage as a function of the input signal envelope. This ensures that the peaking amplifier turns on fully at the peak excursions of the input signal envelope, thereby providing maximum saturated output power.

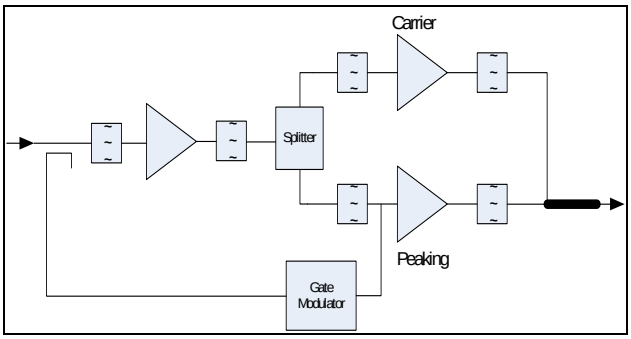

Figure 4: Doherty Amplifier with Gate Modulator and Driver

Table 1 provides a comparison of saturated output power, efficiency at 7.5dB back-off from saturated output power, small signal gain and gain flatness from 2110 to 2170 MHz with and without a gate modulator for the output stage shown in Figure 4. In summary, the gate modulator provides a 1.6dB increase in saturated output power and a 4 point improvement in efficiency at 7.5dB back-off from saturated output power.

Condition	Worst case P_{sat}	Drain Efficiency	Gain	Gain flatness
No GM	53.9dBm, 2.11GHz	42%	14.1dB	0.6dB
With GM	55.5dBm, 2.11GHz	46%	14.0dB	0.7dB

Table 1: Comparison of a Doherty stage P_{sat}, drain efficiency, gain and gain flatness with and without gate modulator.

GaN and LDMOS Comparison

In order to evaluate the latest GaN technology with relation to LDMOS, the following results document in detail the differences and trade-offs. A GaN module (Figure 5) was built that is comprised of a pair of 90W transistors at 2100MHz. It is compared to an LDMOS module (Figure 6) which is comprised of a pair of 100W transistors at 1900MHz. Both of these modules were tuned for efficiency and peak power disregarding the static linearity. The GaN module achieved better efficiency and peak power capability in spite of its higher operating frequency.

	Peak Power	Efficiency
GaN	55.5dBm	50.0% (48.5dBm)
LDMOS	55.2dBm	47% (48.2dBm)

Table 2. Achieved Peak Power and Efficiency

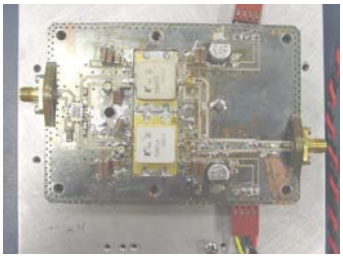

Figure 5. GaN Module

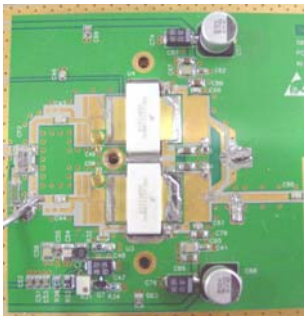

Figure 6. LDMOS Module

With a modulated input signal of 10dB PAR (Peak to Average Ratio) the sampled output signal was captured and analyzed for both modules. The testing revealed that the GaN module exhibits a greater phase compression at output power saturation. This is illustrated by observing the AM-PM plots of Figure 7 and Figure 8. The GaN module compressed by more than 30° at saturation, while the LDMOS module compressed by less than 15° at P_{sat}.

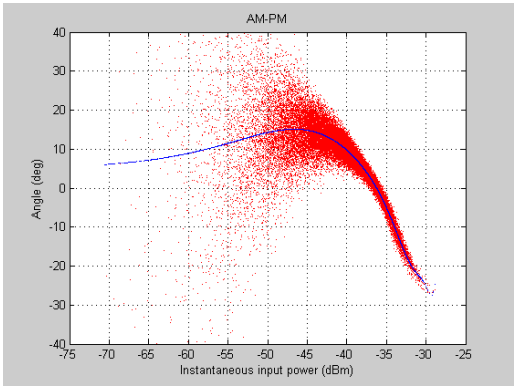

Figure 7. AM-PM GaN Module

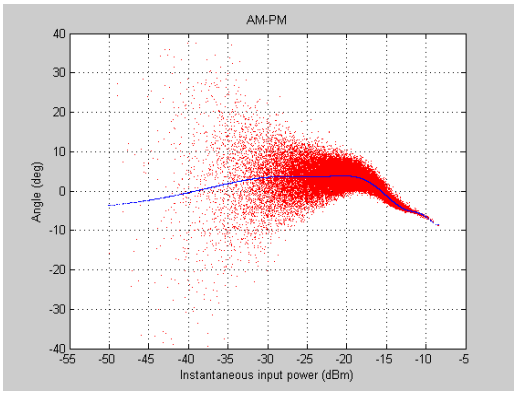

Figure 8. AM-PM LDMOS Module

Using a proprietary technique, the non-linearized EVM (Error Vector Magnitude) was calculated and divided into two components: static and dynamic (memory) EVM

	Static EVM	Memory EVM
GaN	17.5%	4.9%
LDMOS	10.2%	3.1%

Table 3. Error Vector Magnitude

Because of its larger phase compression the GaN module exhibits a larger uncorrected EVM. While the static EVM dominates the linearity of both modules, the dynamic, or memory EVM was also worse for the GaN module.

This may be troublesome for most DPD (digital pre-distortion) linearization methods depending on the modulation BW of the input signal. The LDMOS module exhibited a memory plot with better symmetry.

DPD Results

Spectral plots for linearization of WCDMA carriers for the GaN module are shown in Figure 9 (0110 carrier configuration) and Figure 11 (101 carrier configuration). The 3 plots represent the uncorrected data (black), static correction (green), and memory correction (blue). The results demonstrate that both transistor technologies can

exceed 3GPP requirements at 8.2dB back-off power levels using DPD linearization.

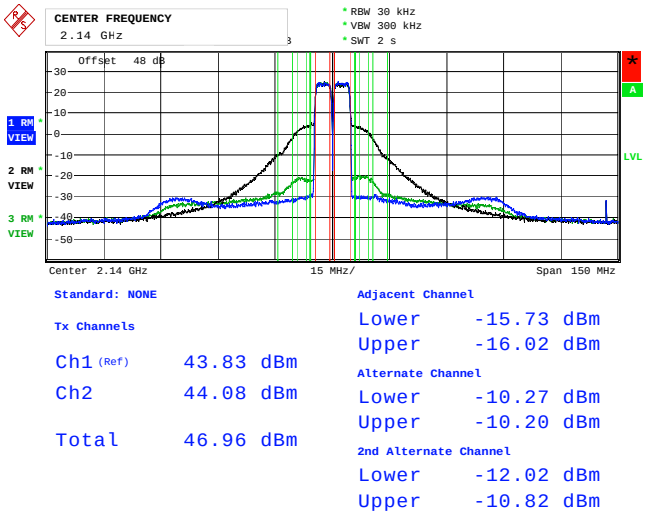

Figure 9. Spectral Measurement GaN Module 0110

A summary chart (Figure 10) reveals that the GaN module struggled to meet 3GPP requirements of -13dBm in a 1MHz integration BW at the lower edge of the 2100MHz downlink band for a 0110 configuration.

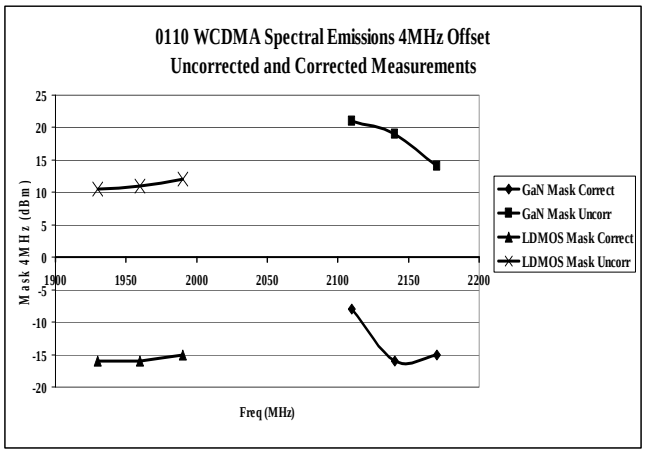

Figure 10. Spectral Mask Summary 0110 Corrected and Uncorrected Data

Comparing the data from the wider BW 101 signal (Figure 11) the narrower band 0110 shows some degradation in performance for the GaN module. Since the LDMOS module is being used as an existing bench mark, the GaN module shows that the correction with narrower band input signal has worse results than the LDMOS module at the lower end of the band.

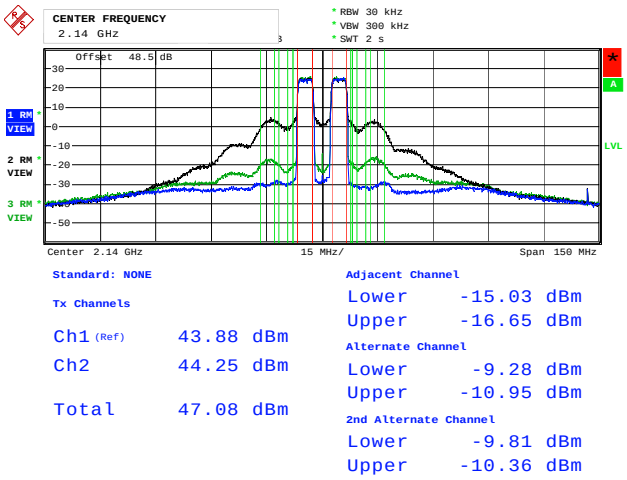

Figure 11. Spectral Measurement GaN Module 101

Observable GaN Advantages

- The GaN module achieved 3% better efficiency over the LDMOS reference module at 7dB operating backoff from P_{Sat}.
- The GaN module demonstrated greater peak power capability and can operate at higher junction temperature.

Observable GaN Disadvantages

- GaN exhibits worse linearity than LDMOS. This may limit the applications where GaN can be utilized for base station applications.
- GaN transistors have a greater cost.

CONCLUSIONS

LDMOS devices have been the technology of choice in use for amplifier architectures used in cellular communication systems. Increasing demands in terms of linearity, cost, efficiency, and higher frequencies of operation are accelerating the development of GaN circuits. Advanced linearization architectures and algorithms are critical as well to the development of future communication systems where high spectral efficiency will be required.

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ACRONYMS

LDMOS: Laterally Diffused Metal Oxide Semiconductor
GaN: Gallium Nitride
FFPA: Feed Forward Power Amplifier
MCPA: Multi-Carrier Power Amplifier
SCPA: Single Carrier Power Amplifier
BTS: Base station Transceiver System