BIAS CIRCUIT TOPOLOGIES FOR MINIMIZATION OF RF AMPLIFIER MEMORY EFFECTS

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Abstract **— Memory effects in amplifiers can be described as the dependence of the output signal not only to the instantaneous input, but also to previous inputs. In a system where these effects exist, the linearity of the amplifier is degraded by the DC supply impedance, which is affected by changes in the instantaneous bandwidth of the input signal. The resulting nonlinearity is difficult to remove completely, even by the most sophisticated predistortion techniques. This paper describes a circuit technique that is readily applicable to RF amplifiers designed for wideband applications used with or without a lineariser. The memory effect reduction is achieved by placing transmission zeros in the bias network transfer function. Transmission zeros at the output of device are formed by utilizing the series resonance properties of decoupling capacitors. The frequency response is synthesized to lower and even out the impedance of the bias network over the resulting distortion bandwidth.**

I. INTRODUCTION

In applications such as UMTS where the modulation bandwidth is large, the video impedance of the dc supply lines to power devices can have an adverse effect on the amplifier performance in terms its efficiency and out of band radiation. The figure of merit to describe the linearity of a PA is the adjacent channel power ratio (ACPR) and is defined as the ratio of a wanted signal power and unwanted distortion generated as a result of amplifier nonlinear transfer characteristics.

In order to contain the output spectrum and the distortion of the PA chain, several linearisation techniques have been employed namely the feedforward (FFWD) system, which is most popular for its wideband performance. As of late, adaptive digital predistortion (ADPD) linearisation has attracted attention for its conformity with digital transmitter architectures. The subject of this paper is related to PA memory effect reduction in general, and in particular in applications where the (RF) amplifier is used in conjunction with digital predistortion linearization, where the most benefit associated with this technique can be achieved. The following section explains the underlying theory.

II. THE THEORY

A frequently used, simplistic representation of an amplifier transfer characteristic is a memory-less function and is given as:

$$i_{out} = g_1 v_{in} + g_2 v_{in}^2 + g_3 v_{in}^3 + g_4 v_{in}^4 + g_5 v_{in}^5 \quad (1)$$

where g_1 - g_n are complex coefficients.

If a two-tone signal of equal amplitude is applied to the input of such a circuit,

$$v_{in} = V_{in} \cdot \cos(\omega_1 t) + V_{in} \cos(\omega_2 t) \quad (2)$$

the 3rd order (IM3) level is given as:

$$IM3 = \frac{3}{4} \cdot g_3 \cdot V_{in}^3 \quad (3)$$

The IM3 sidebands are not a function of input frequency tone spacing, and the distortion level increases in proportion to the 3rd power of the input signal amplitudes. If an RF amplifier behaves accordingly, a digital predistorter can be designed to remove the intermodulation distortion over a wide frequency range (distortion bandwidth). However in practice, the IMD level of a PA normally is a function of modulation bandwidth of the carrier and in a multi-carrier application, the carrier spacing and therefore, the distortion bandwidth has a severe impact on the performance of a predistortion linearisation. This is a direct result of the presence of memory effects.

The memory effects make the IM3 sidebands a function of carrier spacing (distortion bandwidth), and this is attributed to 2nd order nonlinear terms in the amplifier transfer function (equ. 1). The additional distortion is caused by up-conversion of the signal envelope to produce 3rd order IM. Since the nonlinearity of the active device can be modeled as super-position of current sources, the impedance at the device terminal can affect the generated video voltage waveforms (both amplitude and phase). The unconverted IM3 sideband levels are therefore a function of impedance at the envelope frequency that ranges from dc to several tens of MHz and the observed IMD imbalance is due to the phase differences.

The above discussion can be summarized as; if equ. 1 is truncated to the 3rd term, the main contributor to IMD3 is the device 3rd order nonlinearity that is affected by the impedance in carrier RF frequency and remains constant over the frequency range of interest. Nonetheless, the 2nd order nonlinearity (and the associated current source) will also contribute to the IM3 distortion but this contribution is a function of the impedance levels at the envelope frequency. While the DPD can suppress the 3rd order (or even the higher order) nonlinear distortions by producing the inverse of the amplifier transfer function, the predistortion algorithms tends to fail in resolving the memory effects as the cause of this, i.e. the video signal

is an increasing function of frequency. Therefore, the amplifier electrical memory effects are liable for limiting the performance of the digital predistorter.

The dotted-line box in Figure (1) presents a simplified equivalent circuit of the active device, where the 1st, 2nd and 3rd order terms of the transconductance are represented by current sources. It is noted that there are other sources of nonlinearity that are not listed here, but their contributions are considered as being small in magnitude to justify this simplification.

As shown in Fig.1, the device equivalent circuit is connected to two sub-circuits. The RF matching circuit is normally designed to provide the appropriate impedance to the device over the bandwidth of the RF signal. The bias circuit has a low pass response and is responsible for feeding the device with the dc energy, while blocking the RF energy from being wasted in the dc supply network.

The bias line lowpass circuit can be designed using a hybrid of lumped and distributed elements to save real estate. A low pass ladder network is normally formed where the first element looking into the circuit is an inductor. A printed circuit line, often a quarter-wavelength-long at the RF center frequency, can realize this inductor. Quarter wavelength lines are generally preferred as they act as 2nd harmonic traps, which can improve amplifier efficiency. However, shorter lines are also used. The input impedance of such a line if terminated by a low impedance load (shunt capacitor) is approximated by:

$$Z_{in} = jZ_0 \cdot \tan\beta \cdot \ell \qquad (4)$$

Where β ($\beta = 2\pi/\lambda$) is the propagation constant and ℓ is the physical length. Z_0 is the line characteristic impedance. It is clear that as ℓ approaches $\lambda/4$, the input impedance tends to increase very rapidly, providing an open circuit to the RF signal. For the high power PA applications, the width of this (dc feed line) line has to be large and often in excess of tens of milli-inch, reducing the Z_0. As a rule of thumb, the input impedance of the bias line is chosen to be an order of magnitude higher than the impedance looking into the matching circuit at the RF signal frequency. Despite the apparent satisfactory features, this circuit configuration is considered to be the root cause of the electrical memory effect. While the combination described above will have relatively low reactive impedance at the video frequency (several MHz), this impedance is often large enough to create a considerable swing of video voltage in the output terminal of the active device. Moreover, as expected, the magnitude of the video voltage tends to increase with frequency when a current source is loaded with an inductive load and therefore, the IM3 byproducts are frequency dependant too. This additional (frequency dependant) contribution to IM3 is the portion that the DPD linearisers cannot readily remove.

Based on the above outline of the problem, there exist some prior art circuits that reduce the video impedance in a controlled way and improve the amplifier performance. Apart from the techniques published in open literature [1]-[2], the most relevant patent is 5,272,450 by Wisherd. The approach taken by Wisherd provides high RF impedance and low video impedance by forming a series tank resonance (a single pole stop band filter) circuit at the RF frequency using a small inductor in the path of the dc feed. In this fashion, low impedance can be achieved at the video frequency range while blocking the RF current from flowing into the bias supply.

The approach discussed in this paper uses the self-resonance of capacitor(s) used in the bias network to synthesize a prescribed frequency response and a low impedance path for the video signals. In surface mount capacitors, the series inductance is very small and therefore, the resonance frequency is relatively high. A typical circuit showing pair of commercial surface-mount capacitors (0.1μF in parallel with 1μF, ATC 1210 series) is shown in Fig. 2. The self-resonance property of the capacitor can be utilized to design low and almost constant impedance over the video frequency range. Various other circuit topologies may also be used and typical implementations are discussed here.

III. Simulations

In Fig. 2, a circuit configuration is shown that uses a combination of surface mount capacitors and printed inductors to synthesize the desired frequency response in both RF and video frequency ranges. A range of capacitors are used to provide a distributed set of transmission zeros at the video frequencies. In this circuit, the resonance frequencies of C_{18} and C_{19} are chosen to prevent a monotonic increase in the video frequency impedance. Figure 3 illustrates the frequency response of the circuit with and without C_{18} and C_{19}.

The number of transmission zeros can be increased for broadband application by selection of appropriate number of capacitors of right resonance frequency. Fig. 4 shows an alternative configuration. As shown in Fig. 5 a-b, the transmission zeros are spread across the video bandwidth.

Both these configurations also insure that a relatively high impedance level is guaranteed to prevent RF leakage into the dc bias circuit.

IV. Practical Implementation

The bias-decoupling network outlined above was used in a 20W PA in conjunction with digital predistortion and the overall performance of amplifier was improved by 6dB.

References

[1] Bosch W., Gatti G., "Measurement and Simulation of Memory Effects in Predistortion Linearisers", IEEE trans. On MTT, Vol.37, No.12, pp.1885-1890, December 1989.

[2] Vuolevi J H K, et al, "Measurement Technique for Characterizing Memory Effects in RF Power Amplifiers" IEEE Trans. On MTT, Vol. 30 No. 8, 1383-1389, August 2001.

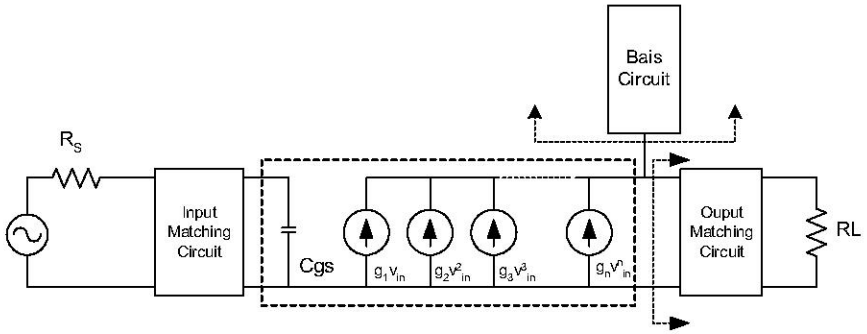


Fig. 1. Typical amplifier circuit representation with nonlinear trans-conductance model.

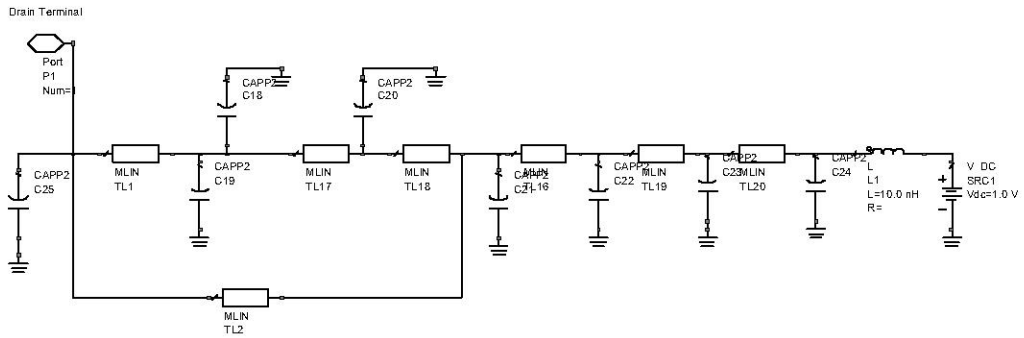


Fig 2. Typical implementation of bias circuitry designed for high power application.

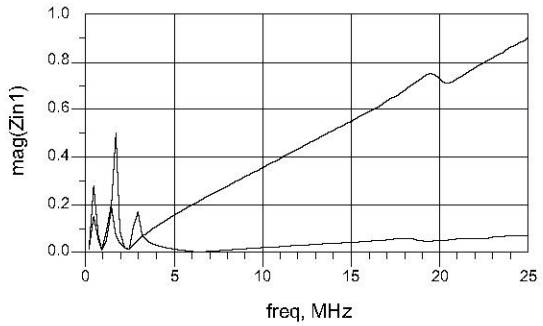


Fig.3. The video impedance of the output network with and without C_{18} and C_{19} decoupling capacitors.

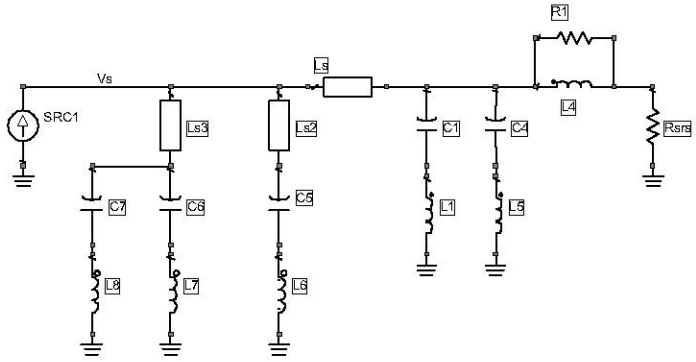
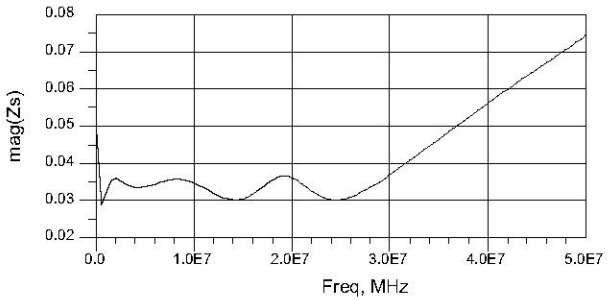
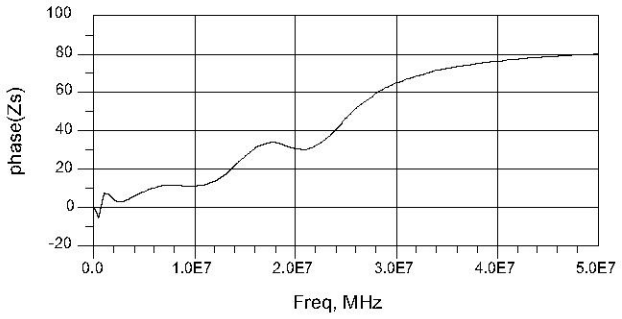


Fig.4. An alternative configuration for drain bias circuit.



(a)



(b)

Fig.5. The magnitude (a) and phase (b) response of the circuit shown in figure 4.